ABSTRACT

A delay circuit including a delay section having two or more predetermined delay stages is disclosed. Each predetermined delay stage adds a predetermined delay time to an input signal. The delay circuit also includes selecting switch sections. At least one of the selecting switch sections includes: a buffer section for receiving a delayed input signal from one of the delay stages and a selecting section means directly connected to the buffer section for activating the buffer section to establish a delay path, wherein an output signal from the delay path has a desired delay time.